Listing of Claims:

1. (Previously Presented) A method of using a computer system to determine an implementation of a user design on a programmable device including a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware, wherein the fixed-configuration secondary hardware has a plurality of inputs, the inputs common to at least two of the programmable logic elements, the method comprising:

for each of a plurality of portions of the user design, determining, with at least one processor of the computer system, one or more sets of input assignments of signals in the user design to the fixed-configuration secondary hardware, each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware;

ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware;

selecting, with the processor, a highest ranked set of input assignments, wherein the highest ranked set is assigned to the fixed-configuration secondary hardware at least two or more times; and

creating, with the processor, an implementation of a subset of the portions of the user design by implementing the selected set of input assignments as inputs to a corresponding subset of the plurality of fixed-configuration secondary hardware.

2. (Previously Presented) The method of claim 1, wherein each of the input assignments defines an assignment of at least one input variable of the user design to an input of the fixed-configuration secondary hardware.

3. (Original) The method of claim 1, wherein the fixed-configuration secondary hardware enables load and clear functions of a register of the programmable device.

4. (Previously Presented) The method of claim 1, wherein each set of the input assignments is associated with at least one register of the user design.

5. (Previously Presented) The method of claim 4, wherein ranking the input assignments includes determining a number of registers of the user design associated with each input assignment.

6. (Previously Presented) The method of claim 5, wherein selecting the highest ranked input assignment includes selecting the input assignment with the most associated registers.

7. (Previously Presented) The method of claim 4, comprising disassociating at least one register from at least one of the input assignments, wherein the disassociated register is associated with the selected input assignment.

8. (Previously Presented) The method of claim 1, comprising removing the selected input assignment from the input assignments, thereby forming a subset of the input assignments.

9. (Previously Presented) The method of claim 8, comprising evaluating a criteria for the subset of the input assignments; and

in response to a determination that the criteria exceeds a threshold, reiterating the steps of ranking the plurality of assignments, and selecting the highest ranked input assignment for the subset of the input assignments.

10. (Previously Presented) The method of claim 2, wherein determining one or more sets of input assignments comprises:

enumerating a plurality of sets of input variables associated with the portion of the user design; and

creating a plurality of input assignments from at least a portion of the sets of input variables.

11. (Previously Presented) The method of claim 10, further comprising:

creating a logic diagram describing the function of each of the plurality of sets of input variables; and

determining from the logic diagram whether the function of each of the plurality of sets of input variables corresponds with at least one function of the fixed-configuration secondary hardware.

12 (Original) The method of claim 11, wherein the logic diagram is a truth table.

13. (Original) The method of claim 11, wherein the logic diagram is a Karnaugh map.

14. (Previously Presented) The method of claim 11, wherein creating a plurality of input assignments comprises applying at least one heuristic to each of the plurality of sets of input variables having a function corresponding with at least one function of the fixed-configuration secondary hardware, thereby determining at least one corresponding assignment.

15. (Original) The method of claim 10, wherein enumerating a plurality of sets of input variables includes using cut enumeration.

16.-19. (Cancelled)

20. (Previously Presented) An information storage medium including instructions adapted to operate an information processing device to perform a set of steps to implement a user design on an integrated circuit, the integrated circuit comprising a plurality of programmable logic elements, each comprising fixed-configuration secondary hardware, the instructions comprising:

for each of a plurality of portions of the user design, determining one or more sets of input assignments of signals in the user design to the fixed-configuration secondary hardware,

each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware;

ranking the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware;

selecting the highest ranked set of input assignments; and

creating, with the processor, an implementation of a subset of the portions of the user design by implementing the selected set of input assignments as inputs to a corresponding subset of the plurality of fixed configuration secondary.

21. (Previously Presented) The information storage medium of claim 20, wherein each of the input assignments defines an assignment of at least one input variable of the user design to an input of the fixed-configuration secondary hardware.

22. (Original) The information storage medium of claim 20, wherein the fixed-configuration secondary hardware enables load and clear functions of a register of the programmable device.

23. (Previously Presented) The information storage medium of claim 20, wherein each set of the input assignments is associated with at least one register of the user design.

24. (Previously Presented) The information storage medium of claim 23, wherein ranking the input assignments includes determining a number of registers of the user design associated with each input assignment.

25. (Previously Presented) The information storage medium of claim 24, wherein selecting the highest ranked input assignment includes selecting the input assignment with the most associated registers.

26. (Previously Presented) The information storage medium of claim 23, comprising disassociating at least one register from at least one of the input assignments, wherein the disassociated register is associated with the selected input assignment.

27. (Previously Presented) The information storage medium of claim 20, comprising removing the selected input assignment from the input assignments, thereby forming a subset of the input assignments.

28. (Previously Presented) The information storage medium of claim 27, comprising evaluating a criteria for the subset of the input assignments; and

in response to a determination that the criteria exceeds a threshold, reiterating the steps of ranking the plurality of assignments and selecting the highest ranked input assignment for the subset of the input assignments.

29. (Previously Presented) The information storage medium of claim 21, wherein determining one or more sets of input assignments comprises:

enumerating a plurality of sets of input variables associated with the portion of the user design; and

creating a plurality of input assignments from at least a portion of the sets of input variables.

30. (Previously Presented) The information storage medium of claim 29, further comprising:

creating a logic diagram describing the function of each of the plurality of sets of input variables; and

determining from the logic diagram whether the function of each of the plurality of sets of input variables corresponds with at least one function of the fixed-configuration secondary hardware.

31. (Original) The information storage medium of claim 30, wherein the logic diagram is a truth table.

32. (Original) The information storage medium of claim 30, wherein the logic diagram is a Karnaugh map.

33. (Previously Presented) The information storage medium of claim 30, wherein creating a plurality of input assignments comprises applying at least one heuristic to each of the plurality of sets of input variables having a function corresponding with at least one function of the fixed-configuration secondary hardware, thereby determining at least one corresponding assignment.

34. (Original) The information storage medium of claim 29, wherein enumerating a plurality of sets of input variables includes using cut enumeration.

35. (Cancelled)

36. (Previously Presented) A method of using a computer system to determine an implementation of a user design on an integrated circuit, the user design comprising a plurality of logic gates and a plurality of registers, the integrated circuit comprising a plurality of programmable logic elements, each programmable logic element comprising a register, a lookup table, and a plurality of logic gates having a plurality of inputs, the method comprising:

for each register in the plurality of registers in the user design, using at least one processor of the computer system in:

determining a logic representation for each of one or more groups of at least one logic gate having a plurality of inputs, the at least one logic gate coupled to the input of the register in the user design;

determining at least one way to implement each logic representation using the plurality of logic gates in a programmable logic element; and

for each way, assigning a set of input signals of the at least one logic gate of the user design to inputs of the logic gates in the programmable logic element; then

for each input signal of a plurality of input signals to the logic gates coupled to input of registers in the user design:

determining, with the processor, a number of occurrences where the input signal is assigned to a same input of the logic gates in a respective programmable logic element;

determining, with the processor, a first input signal and a first input of the logic gates in the programmable logic elements, wherein the first input signal is assigned to the first input more than other input signals are assigned to an input of the logic gates in the programmable logic elements; and then

creating, with the processor, an implementation of the user design on the integrated circuit by implementing the first input signal as the first input of the logic gates in each of the programmable logic elements to which the first input signal was assigned to the first input of the logic gates of that respective programmable logic element.

37. (Previously Presented) The method of claim 36 wherein the logic gates provide load and clear functions for the register in a programmable logic element.